IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Currently Amended) A method of managing power in a graphics controller, comprising:

~~Receiving~~ receiving a change indication related to a system power supply;

~~Adjusting~~ adjusting a first clock;

~~Adjusting~~ adjusting [[a]] the graphics controller power supply voltage level; and

~~Informing~~ informing by the graphics controller a BIOS with an indication of a change related to the system power supply, wherein the informing includes requesting a set of one or more available clock rates.

2. (Canceled)

3. (Currently Amended) The method of claim 2 further comprising:

~~Receiving~~ receiving the set of one or more available clock rates;

~~Checking~~ checking a state of the graphics controller;

~~Choosing~~ choosing a desired clock rate from the set of available clock rates;

~~Adjusting~~ adjusting a second clock to conform to the desired clock rate; and wherein:

~~Adjusting~~ adjusting the first clock comprises reducing a rate of the first clock; and

~~Adjusting~~ adjusting the graphics controller power supply voltage level comprises reducing the graphics controller power supply voltage level.

4. (Currently Amended) The method of claim 3 further comprising:

~~Disabling~~ disabling a CLUT.

5. (Currently Amended) The method of claim 4 wherein:

~~Disabling~~ disabling the CLUT responsive to checking the state of the graphics controller.

6. (Currently Amended) The method of claim 5 further comprising[[:]]

~~Notifying~~ notifying a system to reduce brightness of a display.

7. (Currently Amended) The method of claim 6 wherein[[:]]

~~Notifying~~ notifying the system comprises notifying a chipset directly.

8. (Currently Amended) The method of claim 1 wherein[[:]]

~~The~~ the graphics controller power supply voltage level is associated with a graphics controller power supply internal to the graphics controller.

9. (Currently Amended) The method of claim 2 wherein[[:]]

~~The~~ the graphics controller power supply voltage level is associated with a graphics controller power supply external to the graphics controller, and adjusting the graphics controller power supply voltage level includes programming the graphics controller power supply with a signal.

10. (Currently Amended) The method of claim 1 wherein[[:]]

~~Adjusting~~ adjusting the first clock comprises increasing a rate of the first clock; and

~~Adjusting~~ adjusting the graphics controller power supply voltage level comprises increasing the graphics controller power supply voltage level.

11. (Currently Amended) The method of claim 10 further comprising[[:]]

~~Increasing~~ increasing a clock rate of a second clock.

12. (Currently Amended) The method of claim 11 further comprising[[:]]

~~Enabling~~ enabling a CLUT.

13. (Currently Amended) The method of claim 1 further comprising[[:]]

~~Detecting~~ detecting a change related to a system power supply.

14. (Currently Amended) The method of claim 13 further comprising[[:]]

~~Installing~~ installing a software routine in a system containing the graphics controller, the software routine suitable for detecting the change related to the system power supply.

15. (Currently Amended) A method of effecting power management of a graphics controller in an operating system comprising:

~~Detecting~~ detecting a change in a system power supply;

~~Notifying~~ notifying the graphics controller of the change;

~~Receiving~~ receiving an indication of power reduction in the graphics controller, wherein the receiving the indication includes receiving a request from the graphics controller for a set of available clock frequencies; ~~and~~

~~Providing~~ providing the set of available clock frequencies to the graphics controller, and adjusting a power supply voltage level.

16. (Currently Amended) The method of claim 15 further comprising[[:]]

~~Receiving~~ receiving a signal from the graphics controller to reduce brightness of a display.

17. (Currently Amended) The method of claim 16 further comprising[[:]]

~~Reducing~~ reducing brightness of the display.

18. (Currently Amended) The method of claim 17 further comprising[[:]]

~~Receiving~~ receiving a software routine suitable for notifying the graphics controller, wherein notifying the graphics controller comprises executing the software routine.

19. (Currently Amended) The method of claim 18 further comprising[[:]]

~~Programming~~ programming the set of available clock frequencies and storing the set of the available clock frequencies in a VGA BIOS ("Video Graphics Array Basic Input /Output System").

20. (Currently Amended) The method of claim 3 further comprising[[:]]

~~Disabling~~ disabling a first portion of circuitry of the graphics controller.

21. (Currently Amended) The method of claim 20 wherein

~~Disabling~~ disabling the first portion of circuitry responsive to checking the state of the graphics controller.

22. (Currently Amended) The method of claim 21 further comprising[[:]]

~~Enabling~~ enabling the first portion of circuitry of the graphics controller.

23. (Currently Amended) A graphics controller comprising:

[[A]] a power supply input configured to receive power at a range of voltages from a ~~power~~ voltage regulator;

[[A]] a power supply control output to provide a trigger signal to the ~~power~~ voltage regulator to change the ~~power~~ voltage level supplied to the graphics controller;

[[A]] a first clock, and

~~And~~

[[A]] a system power supply change input.

24. (Currently Amended) The graphics controller of claim 23 further comprising[[:]]

[[A]] a first clock control output.

25. (Currently Amended) The graphics controller of claim 24 further comprising[[:]]

[[A]] a memory coupled to the first clock.

26. (Currently Amended) The graphics controller of claim 24 further comprising[[:]]

[[A]] a second clock; and

[[A]] a second clock control output.

27. (Currently Amended) The graphics controller of claim 26 further comprising[[:]]

[[A]] a memory coupled to the first clock.

28. (Currently Amended) The graphics controller of claim 27 wherein:

~~The~~ the memory is integrated with other portions of the graphics controller on a single substrate.

29. (Currently Amended) The graphics controller of claim 27, wherein ~~further comprising:~~

[[A]] the voltage regulator is coupled to the power supply input and the power supply control output to provide the ~~power~~ voltage to the graphics controller based on the trigger signal from the graphics controller.

30. (Currently Amended) The graphics controller of claim 29 wherein[[:]]

~~The~~ the voltage regulator is integrated with other portions of the graphics controller on a single substrate.

31. (Currently Amended) The graphics controller of claim 30 further comprising[[:]]

[[A]] a VGA BIOS.

32. (Currently Amended) The graphics controller of claim 26 further comprising[[:]]

[[A]] a brightness output configured to signal to a system that a reduction in brightness of a display is appropriate.

33. (Currently Amended) The graphics controller of claim 32 wherein[[:]]

~~The~~ the brightness output is suitable for coupling directly to a video control chipset.

34. (Currently Amended) The graphics controller of claim 32 further comprising[[:]]

[[A]] a 2D engine;

[[A]] a 3D engine;

[[A]] a CLUT coupled to the 3D engine and coupled to the 2D engine;

[[A]] a system interface including the system power supply input;

[[A]] a video interface including the second clock and the second clock control output;

[[A]] a power control interface including the power supply input and the power supply control output;

[[A]] a memory control interface including the first clock; and

[[A]] a control unit coupled to the system interface, the CLUT, the video interface, the power control interface, the memory control interface, the 2D engine and the 3D engine.

35. (Currently Amended) A graphics controller comprising:

[[A]] a power supply input configured to receive power at a range of ~~voltages~~ voltage levels from a power regulator;

[[A]] a power supply control output to provide a trigger signal to the power regulator to change ~~the power~~ a voltage level supplied to the graphics controller;

[[A]] a first clock;

[[A]] a system power supply change input;

[[A]] a first clock control output;

[[A]] a second clock;

[[A]] a second clock control output;

[[A]] a brightness output configured to signal to a system that a reduction in brightness of a display is appropriate;

[[A]] a 2D engine;

[[A]] a 3D engine;

[[A]] a CLUT coupled to the 3D engine and coupled to the 2D engine;

[[A]] a system interface including the system power supply input;

[[A]] a video interface including the second clock and the second clock control output;

[[A]] a power control interface including the power supply input and the power supply control output;

[[A]] a memory control interface including the first clock; and

[[A]] a control unit coupled to the system interface, the CLUT, the video interface, the power control interface, the memory control interface, the 2D engine and the 3D engine.

36. (Currently Amended) A method of managing power in a graphics controller, comprising[[:]]

~~Receiving~~ receiving a change indication related to a system power supply;

reducing a rate of a first clock;

reducing a graphics controller power supply voltage level;

~~Signaling~~ signaling a BIOS with an indication of a change related to the system power supply, wherein the signaling the BIOS includes requesting for a set of one or more available clock rates stored in the BIOS;

~~Receiving~~ receiving a set of one or more available clock rates;

~~Checking~~ checking a state of the graphics controller;

~~Choosing~~ choosing a desired clock rate from the set of available clock rates;

~~Adjusting~~ adjusting a second clock to conform to the desired clock rate;

~~Disabling~~ disabling a first portion of circuitry responsive to checking the state of the graphics controller.